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LSI Logic Corporation  
Legal Department - IP  
1621 Barber Lane, MS D-106  
Milpitas, CA 95035

FAX

Date August 8, 2005Number of pages including cover sheet 2

To: US PTO

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TC 2133

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From: Connie del Castillo

Intellectual Property Paralegal

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## REMARKS:

☐ Urgent☐ For your review☒ Reply ASAP☐ Please comment

Application Number: 10/701,332  
Filing date: November 4, 2003  
First named inventor: Ghassi Agrawal et al.  
Attorney docket number: 03-1343

Transmitted herewith for filing via facsimile:

- Status Request Letter

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PAGE 1/2 \* RCVD AT 8/8/2005 4:55:01 PM [Eastern Daylight Time] \* SVR:USPTO-EFXXF-6/36 \* DNIS:2738300 \* CSID:408 433 7460 \* DURATION (mm-ss):00-34

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## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of :

Ghasi Agrawal et. al.

Serial No. :

10/701,332

Filed :

November 04, 2003

For :Novel BISR Mode to Test the  
Redundant Elements and Regular  
Functional Memory to Avoid Test  
Escapes§  
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§Group Art Unit :

2133

Examiner :Atty Docket :

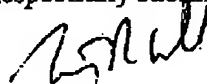
/ 03-1343

STATUS REQUESTCommissioner for Patents  
P. O. Box 1450  
Alexandria, VA 22313-1450

Sir:

Applicants request a status of the above referenced application. Please mail the  
status notification to the address stated below.LSI Logic Corporation  
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[+1] 408-433-7191Date: 8 AUG 05

Respectfully submitted,



Timothy Croll, Ph: [+1] 408-433-7191

Reg. No. 36,771